**LAB 12**

**Objectives:**

**To learn how to design and implement registers and counter using flip flops**

**EQUIPMENT:** Logic trainer, Logic probe

**COMPONENTS**: ICs 74LS08, 74LS32, 74LS04, 74LS86, 74LS02, 74LS74, 74LS153

**REGISTER**:

In this lab, we will design a combinational circuit of register. A register is used to store n bits of information, where n is the number of flip flops. A register consists of a set of flip flops, together with gates that perform data processing tasks. The flip flops hold data, and the gates determine the new or transformed data to be transferred into the flip flops. The registers have two types, one simple register and other register with parallel load. The simple register is discussed above. The register with parallel load is the register in which we can easily store the value of our own choice.

This ability of register is controlled by a control input, if control input is 1 then the data that we want to enter is stored on the register, and when the value is 0 then the data that is already stored in the register remains unchanged. Another type of register is known as shift register.

The shift register is capable of shifting its stored bits laterally in one or both direction. The logical configuration of a shift register consists of a chain of flip flops in cascade, with the output of one flip flop connected to the input of the next flip flop. All flip flops receive a common clock pulse, which activates the shift from each stage to the next.

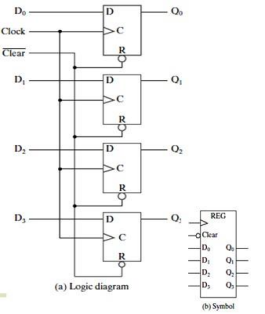
**COUNTERS:**

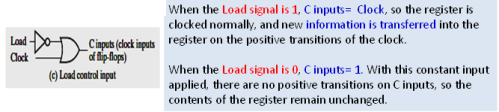
A counter is a register that goes through a predetermined sequence of states upon the application of clock pulses. In a ripple counter, the flip-flop output transition serves as a source for triggering other flip flops. In a synchronous counter, the clock inputs of all of

the flip flops receive the common clock pulse, and the change of state is determined from the present state of the counter.

**Task 1**

Implement a Four-bit register with parallel load using D flip flop.





**Task 2:**

Draw the logic diagram of a shift register with D-FLIP FLOPS with mode selection inputs S1 &S0 and implement the circuit on the logic works. The shift register is to be operated according to following function table. One stage of this register should contain a 4-to-1- line MUX and a D Type FLIP FLOP.

| **Mode Selection** | | **Register Operation** |
| --- | --- | --- |
| **S1** | **S0** |  |
| 0 | 0 | No change |
| 0 | 1 | Shift right |
| 1 | 0 | Shift left |
| 1 | 1 | Parallel load data |

**Task 3**

Implement a 4-bit an asynchronous binary counter with D flip flops. 